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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,615	12/27/2000	Sung-min Yim	AB-1053 US	1304

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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	PAPER NUMBER
2181	9

DATE MAILED: 09/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,615	YIM ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2181	

-- Th MAILING DATE of this communication appears on th cov r sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/752615 .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings were received on 10 September 2003. These drawings are acceptable.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 13 uses cyclic terminology in claiming that the controller activates the second transistor when the second transistor responds to the read control signal. Claim 13 further states that each controller separately activates the associated second transistor by sending a read control signal when cell data of the selected DQ block is

transmitted to the data input/output lines via the first and second transistors, implying that the second transistor is deactivated and is only activated after it is used.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 uses indefinite language in claiming that the controller activates the second transistors of output drivers by sending a read control signal when the second transistors respond to the read control signal, implying that the controllers activate the second transistors when the second transistors respond to the signal from the controllers. Claim 13 further states that each controller separately activates the associated second transistor by sending a read control signal when cell data of the selected DQ block is transmitted to the data input/output lines via the first and second transistors, implying that the second transistor is deactivated and is only activated after it is used to transmit data to the input/output line.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tobin et al. ("Tobin") in view of Gervais et al. ("Gervais").

Tobin teaches all the limitations of Claims 1 and 3 except for the controller including a multiplexer (See Figures 5 and 6, Column 10 Lines 25-67, and Column 11 Lines 1-14 of Tobin). The signal used by the controller to activate the second transistor of Tobin is analogous to the read control signal of Claim 3. Gervais teaches the use of a multiplexer which chooses between two input signals in response to a clock signal in a memory device (See Figure 3, Column 4 Lines 62-67, and Column 5 Lines 1-3 of Gervais). One of ordinary skill in the art at the time the invention was made would construct the controller of Tobin with the clock-controlled multiplexer of Gervais, resulting in the inventions of Claims 1 and 3, in order to allow a signal to be selected from a pair of inputs by a clock signal and provided to the transistor in order to control the rise and fall time (See Column 4 Lines 65-67 of Gervais and Column 10 Lines 25-59 of Tobin).

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tobin and Gervais as applied to Claim 1 above, and further in view of Kametani.

Tobin and Gervais suggest all the features of Claim 2 except deactivating the second transistor when a second set of blocks is selected for data output (See Figures 5 and 6, Column 10 Lines 25-67, and Column 11 Lines 1-14 of Tobin, and Figure 3, Column 4 Lines 62-67, and Column 5 Lines 1-3 of Gervais). Kametani teaches the use of a selective controller which can connect and disconnect one of a plurality of CPUs from a common bus (See Column 10, Lines 28-33 of Kametani). The CPUs of Kametani are analogous to the output driver of Claim 2. One of ordinary skill in the art at the time the invention was made would construct the output driver of Tobin and Gervais with the selective controller of Kametani, resulting in the invention of Claim 2, in order to minimize the capacitive load present on the bus line.

9. Claims 4, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tobin and Gervais as applied to Claim 1 above, and further in view of Garlepp et al. ("Garlepp").

Tobin and Gervais suggest all the features of Claims 4, 5, and 6 except the second transistor being responsive to a read control signal containing calibration information, and the calibration information being comprised of a current and a temperature characteristic (See Figures 5 and 6, Column 10 Lines 25-67, and Column 11 Lines 1-14 of Tobin, and Figure 3, Column 4 Lines 62-67, and Column 5 Lines 1-3 of Gervais). Garlepp teaches a type of memory device, known in the art, which can collect and store a variety of information pertaining to the characteristics of the memory bus, and which can be used to tune the performance of the memory interface. (See Column

3 Lines 47-67 of Garlepp). One of ordinary skill in the art at the time the invention was made would construct the output driver of Tobin and Gervais with the interface taught by Garlepp resulting in the inventions of Claims 4 and 6, in order to tune the performance of the memory interface, as suggested by Garlepp (See Column 3, Lines 65-67 of Garlepp). One of ordinary skill in the art would use the multiplexer of Gervais in the manner discussed in Claim 5 in order to provide a means for selecting the signal to be output by the controller.

10. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham et al. ("Gillingham") in view of Tobin, Gervais and Kametani.

Gillingham teaches the use of a memory subsystem comprising at least two semiconductor devices, a main bus for carrying the data and command information, and an output driver comprised of a single transistor (See Figure 2a, Column 4 Lines 19-22, and Column 6 Lines 19-27 of Gillingham). Gillingham does not teach the use of an output driver comprised of two transistors that can be selectively disconnected from the bus or a multiplexer in the controller choosing between two signals in response to a clock signal. Tobin teaches the use of an output driver comprised of two transistors in which the first transistor is connected to a reference voltage and is responsive to an input signal and the second transistor is connected between the first transistor and the bus and is responsive to a control signal (See Figures 5 and 6, Column 10 Lines 25-67, and Column 11 Lines 1-14 of Tobin). Gervais teaches the use of a multiplexer which chooses between two input signals in response to a clock signal in a memory device

(See Figure 3, Column 4 Lines 62-67, and Column 5 Lines 1-3 of Gervais). Kametani teaches the use of a controller that can selectively connect and disconnect CPUs from a bus line (See Column 10, Lines 28-33 of Kametani). The CPUs of Kametani are analogous to the output drivers of Claim 7. One of ordinary skill in the art at the time the invention was made would construct the memory system of Gillingham with the output driver of Tobin, the clock-controlled multiplexer of Gervais, and the selective controller of Kametani, resulting in the inventions of Claim 7 and 9, in order to minimize the capacitance of the bus line, which in turn will minimize the power consumed by the device as well as minimize the degradation of the data being transmitted across the bus. One of ordinary skill in the art would use the multiplexer of Gervais in the manner discussed in Claim 9 in order to provide a means for selecting the signal to be output by the controller.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, Tobin, Gervais and Kametani as applied to Claim 7 above, and further in view of Kohno.

Gillingham, Tobin, Gervais, and Kametani teach all the limitations of Claim 8 except the second transistors of all the output drivers being simultaneously activated (See Figure 2a, Column 4 Lines 19-22, and Column 6 Lines 19-27 of Gillingham; Figures 5 and 6, Column 10 Lines 25-67, and Column 11 Lines 1-14 of Tobin; Figure 3, Column 4 Lines 62-67, and Column 5 Lines 1-3 of Gervais; and Column 10 Lines 28-33 of Kametani). Kohno teaches a semiconductor memory device in which all of the

memory modules are simultaneously activated during a read operation (See Column 11 Lines 66-67 and Column 12 Lines 1-3 of Kohno). One of ordinary skill in the art at the time the invention was made would combine the memory module of Gillingham, Tobin, Gervais, and Kametani with the memory module of Kohno, resulting in the invention of Claim 8, in order to produce a device which will send all read-out data to an external element simultaneously, as discussed in Kohno (See Column 11 Lines 61-65 of Kohno).

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, Tobin, Gervais, and Kametani as applied to Claim 7 above, and further in view of Garlepp.

Gillingham, Tobin, Gervais, and Kametani teach all the limitations of Claim 10 except for the characteristics of the data input/output line being an output current characteristic and a temperature characteristic (See Figure 2a, Column 4 Lines 19-22, and Column 6 Lines 19-27 of Gillingham; Figures 5 and 6, Column 10 Lines 25-67, and Column 11 Lines 1-14 of Tobin; Figure 3, Column 4 Lines 62-67, and Column 5 Lines 1-3 of Gervais; and Column 10 Lines 28-33 of Kametani). Garlepp teaches a type of memory device, known in the art, which can collect and store a variety of information pertaining to the characteristics of the memory bus, and which can be used to tune the performance of the memory interface. (See Column 3 Lines 47-67 of Garlepp). One of ordinary skill in the art at the time the invention was made would construct the output driver of Tobin et al. with the interface taught by Garlepp et al. resulting in the invention

of Claim 10, in order to tune the performance of the memory interface, as suggested by Garlepp et al. (See Column 3, Lines 65-67 of Garlepp).

13. Claims 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham in view of Tobin, Gervais, and Garlepp.

Gillingham teaches the use of a memory system comprising a plurality of memory devices and a plurality of output drivers comprised of a single transistor and a controller. Gillingham does not teach the use of an output driver comprised of two transistors, a multiplexer in the controller choosing between two signals in response to a clock signal, or the second transistor being responsive to a read control signal containing calibration information, said calibration information being comprised of a current and a temperature characteristic (See Figure 2a; Column 4, Lines 19-22; and Column 6 Lines 19-27 of Gillingham). Tobin teaches the use of an output driver comprised of two transistors in which the first transistor is connected to a reference voltage and is responsive to an input signal and the second transistor is connected between the first transistor and the bus and is responsive to a control signal (See Figures 5 and 6, Column 10 Lines 25-67, and Column 11 Lines 1-14 of Tobin). Garlepp teaches a type of memory device, known in the art, which can collect and store a variety of information pertaining to the characteristics of the memory bus, and which can be used to tune the performance of the memory interface. (See Column 3 Lines 47-67 of Garlepp). One of ordinary skill in the art at the time the invention was made would construct the memory system of Gillingham with the output driver of Tobin, the clock-

controlled multiplexer of Gervais, and the interface taught by Garlepp resulting in the inventions of Claims 11, 14, and 15, in order to tune the performance of the memory interface, as suggested by Garlepp (See Column 3, Lines 65-67 of Garlepp) and to minimize the capacitance of the bus line, which in turn will minimize the power consumed by the device as well as minimize the degradation of the data being transmitted across the bus. One of ordinary skill in the art would use the multiplexer of Gervais in the manner discussed in Claim 14 in order to provide a means for selecting the signal to be output by the controller.

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, Tobin, Gervais, and Garlepp in further view of Kametani.

Gillingham, Tobin, Gervais, and Garlepp teach all the restrictions of Claim 12 except for deactivation the second transistors of the output drivers in unselected blocks (See Figure 2a, Column 4 Lines 19-22, and Column 6 Lines 19-27 of Gillingham; Figures 5 and 6, Column 10 Lines 25-67, and Column 11 Lines 1-14 of Tobin; Figure 3, Column 4 Lines 62-67, and Column 5 Lines 1-3 of Gervais; and Column 3 Lines 65-67 of Garlepp). Kametani teaches the use of a controller that can selectively connect and disconnect CPUs from a bus line (See Column 10 Lines 28-33 of Kametani). The CPUs of Kametani are analogous to the second transistors of the output drivers of Claim 12. One of ordinary skill in the art at the time the invention was made would combine the semiconductor memory device of Gillingham, Tobin, Gervais, and Garlepp with the

controller of Kametani, resulting in the invention of Claim 12, in order to minimize the capacitive load on the bus line.

Response to Arguments

15. Applicant's arguments with respect to Claims 1-15 have been considered but are moot in view of the new ground(s) of rejection. Applicant has modified the scope of the claims to include a multiplexer in the controller. As shown above, such changes are not persuasive to overcome a rejection based on 35 U.S.C. 103(a). The new ground(s) of rejection presented in this Office action in reference to the aforementioned claims have been necessitated by the Applicant's amendment.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

tjc